ASPLOS-VI
Advance Program

Sixth International Conference on
Architectural Support for Programming Languages and Operating Systems
October 4-7, 1994 San Jose, California

Tuesday, October 4

First Workshop on Networks of Workstations (NOW)

Tom Anderson and Dave Patterson, *Univ. of California, Berkeley*

Desktop computers offer the promise of being the new building block for large-scale computers of the future. By leveraging the improving cost/performance of complete systems—workstation hardware and software—with the emerging switch-based local area networks, networks of workstations (NOWs) may be the successors to today's massively parallel processors, mainframes, and shared bus multiprocessor servers.

This first NOW workshop will address four key issues for NOW. The format is to have speakers give short talks. These will be followed by a panel session led by an "instigator," with plenty of breaks for discussions. Following ASPLOS traditions, there will be speakers covering hardware and software from industry and academia. The tentative outline for the one-day workshop is:

- **Interconnects for NOW**
  John Hennessy, *Stanford Univ.*
- **What's the Programming Model NOW?**
  Mark Hill, *Univ. of Wisconsin*
- **Getting the Operating System out of the Way**
  Marc Weiser, *Xerox PARC*
- **Who Cares? (NOW Applications)**
  Jim Gray, *DEC*

Tuesday Evening, October 4

ASPLOS-VI Reception

An informal gathering for conference and workshop attendees.

Wednesday, October 5

Welcome and Keynote Address

Session I: Operating System Issues

- *Separating Data and Control Transfer in Distributed Operating Systems*, Chandramohan A. Thekkath, Henry M. Levy, and Edward D. Lazowska (Univ. of Washington)
- *Scheduling and Page Migration for Multiprocessor Compute Servers*, Rohit Chandra, Scott Devine, Ben Verghese, Anoop Gupta, and Mendel Rosenblum (Stanford Univ.)
- *Reactive Synchronization Algorithms for Multiprocessors,* Beng-Hong Lim and Anant Agarwal (MIT)

Session II: Communication in Parallel Machines

- *Integration of Message Passing and Shared Memory in the Stanford FLASH Multiprocessor*, John Heinlein, Kourosh Gharachorloo, Scott A. Dresser, and Anoop Gupta (Stanford Univ.)
- *Software Overhead in Messaging Layers: Where Does the Time Go?*, Vijay Karamcheti and Andrew A. Chien (Univ. of Illinois)
- *Where is Time Spent in Message Passing and Shared Memory Programs?*, Satish Chandra, James R. Larus (Univ. of Wisconsin), and Anne Rogers (Princeton Univ.)

Session III: Hardware Topics

- *Performance of a Hardware-Assisted Real-Time Garbage Collector*, William J. Schmidt (IBM) and Kelvin D. Nilsen (Iowa State)
- *eNVy: A Non-Volatile, Main Memory Storage System*, Michael Wu and Willy Zwaenepoel (Rice Univ.)
- *Resource Allocation in a High Clock Rate Microprocessor*, Michael Upton, Thomas Huff, Trevor Mudge, and Richard Brown (Univ. of Michigan)
- *Hardware and Software Support for Efficient Exception Handling*, Chandramohan A. Thekkath and Henry M. Levy (Univ. of Washington)

Wednesday Evening, October 5

Evening Panel Session and Open Bar

One panel session will be held during ASPLOS-VI. As is customary, it will be on a controversial and topical subject.

Thursday, October 6

Session IV: Instrumentation and Measurement

- *A Technique for Monitoring Run-time Dynamics of an Operating System and a Microprocessor Executing User Applications*, Pramod V. Argade, David K. Charles (AT&T Bell Labs), and Craig Taylor (EO Inc.)
- *Trap-driven Simulation with Tapeworm II,* Richard Uhlig, David Nagle, Trevor Mudge, and Stuart Sechrest (Univ. of Michigan)
- *Contrasting Characteristics and Cache Performance of Technical and Multi-User Commercial Workloads*, Ann Marie Grizzaffi Maynard, Colette M. Donnelly, and Bret R. Olszewski (IBM)

Session V: Uniprocessor Performance Issues

- *Avoiding Conflict Misses Dynamically in Large Direct-Mapped Caches*, Brian N. Bershad, Dennis Lee, Theodore H. Romer (Univ. of Washington), and J. Bradley Chen (CMU)
- *Surpassing the TLB Performance of Superpages with Less Operating System Support*, Madhusudhan Talluri and Mark D. Hill (Univ. of Wisconsin)
- *Dynamic Memory Disambiguation Using the Memory Conflict Buffer,* David M. Gallagher, William Y. Chen, Scott A. Mahlke, John C. Gyllenhaal, and Wen-mei W. Hwu (Univ. of Illinois)

Session VI: Language and Architecture

- *AP1000+: Architectural Support of PUT/GET Interface for Parallelizing Compiler*, Kenichi Hayashi, Tunehisa Doi, Takeshi Horie, Yoichi Koyanagi, Osamu Shiraki, Nobutaka Imamura, Toshiyuki Shimizu, Hiroaki Ishihata, and Tatsuya Shindo (Fujitsu Labs)
- *LCM: Memory System Support for Parallel Language Implementation*, James R. Larus, Brad Richards, and Guhan Viswanathan (Univ. of Wisconsin)
- *The Performance Advantages of Integrating Block Data Transfer in Cache-Coherent Multiprocessors*, Steven Cameron Woo, Jaswinder Pal Singh, and John L. Hennessy (Stanford Univ.)

Session VII: Code Transformation

- *Improving the Accuracy of Static Branch Prediction Using Branch Correlation*, Cliff Young and Michael D. Smith (Harvard Univ.)
- *Reducing Branch Costs via Branch Alignment*, Brad Calder and Dirk Grunwald (Univ. of Colorado)
- *Compiler Optimizations for Improving Data Locality,* Steve Carr (Michigan Tech.), Kathryn S. McKinley (Univ. of Mass.), and Chau-Wen Tseng (Stanford Univ.)
- *DCG: An Efficient, Retargetable Dynamic Code Generation System*, Dawson R. Engler (MIT) and Todd A. Proebsting (Univ. of Arizona)

Friday, October 7

Session VIII: Memory Access in Shared-Memory Multiprocessors

- *The Performance Impact of Flexibility in the Stanford FLASH Multiprocessor*, Mark Heinrich, Jeffrey Kuskin, David Ofelt, John Heinlein, Jaswinder Pal Singh, Richard Simoni, Kourosh Gharachorloo, Joel Baxter, David Nakahira, Mark Horowitz, Anoop Gupta, Mendel Rosenblum, and John Hennessy (Stanford Univ.)
- *Simple Compiler Algorithms to Reduce Ownership Overhead in Cache Coherence Protocols*, Jonas Skeppstedt and Per Stenstrom (Lund Univ.)
- *Fine-grain Access Control for Distributed Shared Memory,* Ioannis Schoinas, Babak Falsafi, Alvin R. Lebeck, Steven K. Reinhardt, James R. Larus, and David A. Wood (Univ. of Wisconsin)

Session IX: Multithreading

- *Interleaving: A Multithreading Technique Targeting Multiprocessors and Workstations*, James Laudon (Silicon Graphics), Anoop Gupta, and Mark Horowitz (Stanford Univ.)
- *Hardware Support for Fast Capability-Based Addressing*, Nicholas P. Carter, Stephen W. Keckler, and William J. Dally (MIT)
- *The Effectiveness of Multiple Hardware Contexts*, Radhika Thekkath and Susan J. Eggers (Univ. of Washington)

Conference Chairs

General	Forest Baskett, *Silicon Graphics*
Program	Douglas Clark, *Princeton Univ.*
Treasurer	Robert Swedroe, *MIPS Technologies*
Publicity	Kunle Olukotun, *Stanford Univ.*
	Darlene Hadding, *Stanford Univ.*
Local Arrangements	Melissa Anderson, *Silicon Graphics*
Registration	Melissa Anderson, *Silicon Graphics*

Program Committee

Anant Agarwal	*MIT*
Brian Bershad	*Univ. of Washington*
Anita Borg	*DEC Network Systems Lab*
David E. Culler	*Univ. of Calif., Berkeley*
Susan Eggers	*Univ. of Washington*
Carla Ellis	*Duke Univ.*
Josh Fisher	*HP Labs*
Mark D. Hill	*Univ. of Wisconsin-Madison*
Wen-mei Hwu	*Univ. of Illinois*
Monica Lam	*Stanford Univ.*
Susan Owicki	*Consultant*
Michael Powell	*Sun Microsystems Labs*
Anne Rogers	*Princeton Univ.*
Margo Seltzer	*Harvard Univ.*
Jim Smith	*Cray Research*
Mary Lou Soffa	*Univ. of Pittsburgh*

Conference Site and Accommodation

All technical sessions, lunches, and registration will be held at the Fairmont Hotel. Contact the hotel directly for reservations and indicate ASPLOS-VI conference. Conference rates are $107 per night for single or double room (10% city occupancy tax not included). Reservations must be received by **September 4, 1994**, to guarantee conference rate. Late reservations will be accepted on a space-available basis.

The Fairmont Hotel is conveniently located in Downtown San Jose. It is adjacent to the city's light-rail transit line and is within walking distance of theaters, museums, civic buildings, and Center of Performing Arts.

Fairmont Hotel At Fairmont Plaza
170 South Market Street
San Jose, CA 95113-2395
1-800-527-4727 or (408) 998-1900
Fax (408) 280-0394

Air Transportation

San Jose International Airport is located near the Fairmont Hotel. Special arrangements have been made with Thomas Cook Travel of San Francisco, California, to provide conference attendees with the lowest round-trip fare without staying over Saturday night. To take advantage of this offer, contact Thomas Cook Travel at 1-800-648-MEET (1-800-648-6338) and mention "ASPLOS-VI."

Ground Transportation

The Fairmont Hotel is less than 10 minutes from the San Jose International Airport. There is complimentary shuttle service to and from the airport: Weekdays, 5:30 a.m. to 11 p.m., and Weekends, 7 a.m. to 11 p.m. Taxi fare is approximately $6 one way.

Weather

San Jose is known for its comfortable climate. In October the day-time temperature is usually 70°-80°F and evening temperatures are 50°-60°F. Rain is not likely. A jacket will probably be needed. Casual attire is appropriate throughout the conference.

Registration

Early registration must be postmarked by **August 26, 1994**. A T-shirt is included with early registration. Full payment in U.S. dollars must accompany registration: check drawn from a U.S. bank or charge to a MasterCard or Visa card. Credit card registration may be faxed to (415) 969-6289 — Attn: Melissa Anderson. Conference registration includes one copy of the proceedings, lunches, breaks, and receptions. Registration for the workshop session includes one copy of notes, lunch, and breaks. The student registration fee excludes meals; traditionally, regular ASPLOS attendees who do not plan to use their meal tickets normally donate them to students. Student registration must include a copy of a valid, full-time student ID.

A copy of this form may be retrieved by anonymous ftp from *max.stanford.edu,* file *pub/ASPLOS-VI/adv.prgm*. For further information, contact Melissa Anderson at asplos6@sgi.com.

Register early for a free ASPLOS T-Shirt.

ASPLOS-VI Registration Form

October 4-7, 1994 San Jose, California

Name .....

Affiliation .....

Address .....

.....

Telephone .....

Fax .....

Electronic Mail Address .....

☐ ACM ☐ IEEE Member No. .....

Please list any special needs or accommodations:

(Before Aug. 26)	Member	Non-Member	Student*
Conference	☐ $295	☐ $413	☐ $120
Workshop	☐ $100	☐ $140	☐ $75
T-Shirt Size	☐ Medium	☐ Large	☐ X-Large

T-Shirt included with registration postmarked by Aug. 26 only.

(After Aug. 26)			
Conference	☐ $398	☐ $558	☐ $120
Workshop	☐ $135	☐ $189	☐ $75

* Student registration must be accompanied by a copy of a valid, full-time student ID; meals not included.

☐ Check drawn on U.S. bank payable to: **ASPLOS-VI**
☐ MasterCard ☐ Visa

Card No. .....

Expiration Date .....

Name on Card .....

Signature .....

Send Registration Form With Payment To:

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Silicon Graphics, Inc.
2100 North Shoreline Boulevard
M/S 6L-005
Mountain View, CA 94043
Fax:(415) 969-6289

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