Final Program

ASPLOS-VI

Sixth International Conference on

October 4-7, 1994
San Jose, California

SIGARCH
SIGPLAN
SIGOPS

Sponsored by the ACM
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ASPLOS-VI

Registration Schedule

Outside Imperial Ballroom

Monday, October 3, 1994
5:30 p.m. - 7:30 p.m.

Tuesday, October 4, 1994
7:30 a.m. - 5:30 p.m.

Wednesday, October 5, 1994
7:30 a.m. - 5:30 p.m.

Thursday, October 6, 1994
7:30 a.m. - 5:30 p.m.

Friday, October 7, 1994
8:30 a.m. - 10:30 a.m.

Workshop

Tuesday, October 4, 1994
8:30 a.m. - 6:30 p.m.
Regency Ballroom

Reception

Tuesday, October 4, 1994
7:00 p.m. - 9:00 p.m.
The Tech Museum of Innovation
145 West San Carlos Street
(walking distance from the Fairmont)

Evening Panel Session

Wednesday, October 5, 1994
7:30 p.m. - 9:30 p.m.
Imperial Ballroom

Technical Sessions

Wednesday - Friday
October 5 - 7, 1994
Imperial Ballroom

Tuesday, October 4, 1994

(All sessions in the Regency Ballroom)

First Workshop on Networks of Workstations (NOW)

Co-Chairs: Tom Anderson and Dave Patterson, *Univ. of California, Berkeley*

Desktop computers offer the promise of being the new building block for large-scale computers of the future. By leveraging the improving cost/performance of complete systems—workstation hardware and software—with the emerging switch-based local area networks, networks of workstations (NOWs) may be the successors to today's massively parallel processors, mainframes, and shared bus multiprocessor servers.

This first NOW workshop will address five key issues for NOW. Each session will have two or three speakers giving short talks. These will be followed by a panel session led by an "instigator," with plenty of breaks for discussions. Following ASPLOS traditions, speakers will be covering hardware and software from industry and academia.

Morning

8:30 Session 1: Interconnects for NOW

Instigator: John Hennessy, *Stanford Univ.*
Speakers: Chuck Seitz, *Myricom*
Greg Papadopoulos, *Thinking Machines*
Gaurav Garg, *Synoptics*

Break

10:30 Session 2: What's the Programming Model NOW?

Instigator: Mark Hill, *Univ. of Wisconsin*
Speakers: Kai Li, *Princeton Univ.*
Anoop Gupta, *Stanford Univ.*
David Culler, *Univ. of California, Berkeley*

Afternoon

12:00 Lunch

1:15 Session 3: Getting the Operating System Out of the Way

Instigator: Brian Bershad, *Univ. of Washington*
Speakers: Tom Anderson, *Univ. of California, Berkeley*
Frans Kaashoek, *MIT*
Larry Peterson, *Univ. of Arizona*

Break

3:15 Session 4: Who Cares? (About Applications)

Instigator: Jim Gray, *DEC*
Speakers: Bill Farrell, *SAIC*
Rick Rashid, *Microsoft*
Willy Zwaenepoel, *Rice Univ.*

Break

5:15 Session 5: Perspective: Whither NOW?

Instigator: Marc Weiser, *Xerox PARC*
Speakers: Ed Lazowska, *Univ. of Washington*
Dave Patterson, *Univ. of California, Berkeley*

6:30 Adjourn to ASPLOS-VI Reception

Evening

7:00-9:00 ASPLOS-VI Reception (The Tech Museum)

An informal gathering for conference and workshop attendees.

Wednesday, October 5, 1994

(All sessions in the Imperial Ballroom)

Morning

9:00-10:00 Welcome and Keynote Address

Randy Katz, *ARPA and Univ. of California, Berkeley*

10:00-10:30 Break (outside Imperial Ballroom)

10:30-12:00 Session I: Operating System Issues

Chair: Margo Seltzer, *Harvard Univ.*

- *Separating Data and Control Transfer in Distributed Operating Systems*, Chandramohan A. Thekkath, Henry M. Levy, and Edward D. Lazowska (Univ. of Washington)
- *Scheduling and Page Migration for Multiprocessor Compute Servers*, Rohit Chandra, Scott Devine, Ben Verghese, Anoop Gupta, and Mendel Rosenblum (Stanford Univ.)
- *Reactive Synchronization Algorithms for Multiprocessors*, Beng-Hong Lim and Anant Agarwal (MIT)

Afternoon

12:00-1:30 Lunch (outside Imperial Ballroom)

1:30-3:00 Session II: Communication in Parallel Machines

Chair: Susan Owicki, *Consultant*

- *Integration of Message Passing and Shared Memory in the Stanford FLASH Multiprocessor*, John Heinlein, Kourosh Gharachorloo, Scott A. Dresser, and Anoop Gupta (Stanford Univ.)
- *Software Overhead in Messaging Layers: Where Does the Time Go?*, Vijay Karamcheti and Andrew A. Chien (Univ. of Illinois)
- *Where is Time Spent in Message Passing and Shared Memory Programs?*, Satish Chandra, James R. Larus (Univ. of Wisconsin), and Anne Rogers (Princeton Univ.)

3:00-3:30 Break (outside Imperial Ballroom)

3:30-5:30 Session III: Hardware Topics

Chair: Jim Smith, *Univ. of Wisconsin*

- *Performance of a Hardware-Assisted Real-Time Garbage Collector*, William J. Schmidt (IBM) and Kelvin D. Nilsen (Iowa State)
- *eNVy: A Non-Volatile, Main Memory Storage System*, Michael Wu and Willy Zwaenepoel (Rice Univ.)
- *Resource Allocation in a High Clock Rate Microprocessor*, Michael Upton, Thomas Huff, Trevor Mudge, and Richard Brown (Univ. of Michigan)
- *Hardware and Software Support for Efficient Exception Handling*, Chandramohan A. Thekkath and Henry M. Levy (Univ. of Washington)

Evening

7:30-9:30 Evening Panel Session and Open Bar
(Session in the Imperial Ballroom)

"Whither Computer Architecture: Does PLOS Need AS?"

Thursday, October 6, 1994

(All sessions in the Imperial Ballroom)

Morning

8:30-10:00 Session IV: Instrumentation and Measurement

Chair: Susan Eggers, *Univ. of Washington*

- *A Technique for Monitoring Run-time Dynamics of an Operating System and a Microprocessor Executing User Applications*, Pramod V. Argade, David K. Charles (AT&T Bell Labs), and Craig Taylor (EO Inc.)
- *Trap-driven Simulation with Tapeworm II,* Richard Uhlig, David Nagle, Trevor Mudge, and Stuart Sechrest (Univ. of Michigan)
- *Contrasting Characteristics and Cache Performance of Technical and Multi-User Commercial Workloads*, Ann Marie Grizzaffi Maynard, Colette M. Donnelly, and Bret R. Olszewski (IBM)

10:00-10:30 Break (outside Imperial Ballroom)

10:30-12:00 Session V: Uniprocessor Performance Issues

Chair: Anne Rogers, *Princeton Univ.*

- *Avoiding Conflict Misses Dynamically in Large Direct-Mapped Caches*, Brian N. Bershad, Dennis Lee, Theodore H. Romer (Univ. of Washington), and J. Bradley Chen (CMU)
- *Surpassing the TLB Performance of Superpages with Less Operating System Support*, Madhusudhan Talluri and Mark D. Hill (Univ. of Wisconsin)
- *Dynamic Memory Disambiguation Using the Memory Conflict Buffer,* David M. Gallagher, William Y. Chen, Scott A. Mahlke, John C. Gyllenhaal, and Wen-mei W. Hwu (Univ. of Illinois)

Afternoon

12:00-1:30 Lunch (outside Imperial Ballroom)

1:30-3:00 Session VI: Language and Architecture

Chair: Brian Bershad, *Univ. of Washington*

- *AP1000+: Architectural Support of PUT/GET Interface for Parallelizing Compiler*, Kenichi Hayashi, Tunehisa Doi, Takeshi Horie, Yoichi Koyanagi, Osamu Shiraki, Nobutaka Imamura, Toshiyuki Shimizu, Hiroaki Ishihata, and Tatsuya Shindo (Fujitsu Labs)
- *LCM: Memory System Support for Parallel Language Implementation*, James R. Larus, Brad Richards, and Guhan Viswanathan (Univ. of Wisconsin)
- *The Performance Advantages of Integrating Block Data Transfer in Cache-Coherent Multiprocessors*, Steven Cameron Woo, Jaswinder Pal Singh, and John L. Hennessy (Stanford Univ.)

3:00-3:30 Break (outside Imperial Ballroom)

3:30-5:30 Session VII: Code Transformation

Chair: Monica Lam, *Stanford Univ.*

- *Improving the Accuracy of Static Branch Prediction Using Branch Correlation*, Cliff Young and Michael D. Smith (Harvard Univ.)
- *Reducing Branch Costs via Branch Alignment*, Brad Calder and Dirk Grunwald (Univ. of Colorado)
- *Compiler Optimizations for Improving Data Locality,* Steve Carr (Michigan Tech.), Kathryn S. McKinley (Univ. of Mass.), and Chau-Wen Tseng (Stanford Univ.)
- *DCG: An Efficient, Retargetable Dynamic Code Generation System*, Dawson R. Engler (MIT) and Todd A. Proebsting (Univ. of Arizona)

Friday, October 7, 1994

(All sessions in the Imperial Ballroom)

Morning

8:30-10:00 Session VIII: Memory Access in Shared-Memory Multiprocessors

Chair: Wen-Mei Hwu, *Univ. of Illinois*

- *The Performance Impact of Flexibility in the Stanford FLASH Multiprocessor*, Mark Heinrich, Jeffrey Kuskin, David Ofelt, John Heinlein, Jaswinder Pal Singh, Richard Simoni, Kourosh Gharachorloo, Joel Baxter, David Nakahira, Mark Horowitz, Anoop Gupta, Mendel Rosenblum, and John Hennessy (Stanford Univ.)
- *Simple Compiler Algorithms to Reduce Ownership Overhead in Cache Coherence Protocols*, Jonas Skeppstedt and Per Stenstrom (Lund Univ.)
- *Fine-grain Access Control for Distributed Shared Memory,* Ioannis Schoinas, Babak Falsafi, Alvin R. Lebeck, Steven K. Reinhardt, James R. Larus, and David A. Wood (Univ. of Wisconsin)

10:00-10:30 Break (outside Imperial Ballroom)

10:30-12:00 Session IX: Multithreading

Chair: Mark Hill, *Univ. of Wisconsin*

- *Interleaving: A Multithreading Technique Targeting Multiprocessors and Workstations*, James Laudon (Silicon Graphics), Anoop Gupta, and Mark Horowitz (Stanford Univ.)
- *Hardware Support for Fast Capability-Based Addressing*, Nicholas P. Carter, Stephen W. Keckler, and William J. Dally (MIT)
- *The Effectiveness of Multiple Hardware Contexts*, Radhika Thekkath and Susan J. Eggers (Univ. of Washington)

Conference Chairs

General	Forest Baskett, *Silicon Graphics*
Program	Douglas Clark, *Princeton Univ.*
Treasurer	Robert Swedroe, *MIPS Technologies*
Publicity	Kunle Olukotun, *Stanford Univ.* Darlene Hadding, *Stanford Univ.*
Local Arrangements	Melissa Anderson, *Silicon Graphics*
Registration	Melissa Anderson, *Silicon Graphics*

Program Committee

Anant Agarwal	*MIT*
Brian Bershad	*Univ. of Washington*
Anita Borg	*DEC Network Systems Lab*
David E. Culler	*Univ. of California, Berkeley*
Susan Eggers	*Univ. of Washington*
Carla Ellis	*Duke Univ.*
Josh Fisher	*HP Labs*
Mark D. Hill	*Univ. of Wisconsin-Madison*
Wen-mei Hwu	*Univ. of Illinois*
Monica Lam	*Stanford Univ.*
Susan Owicki	*Consultant*
Michael Powell	*Sun Microsystems Labs*
Anne Rogers	*Princeton Univ.*
Margo Seltzer	*Harvard Univ.*
Jim Smith	*Cray Research*
Mary Lou Soffa	*Univ. of Pittsburgh*

Registration

Conference registration includes one copy of the proceedings, lunches, breaks, and receptions. Registration for the workshop session includes one copy of notes, lunch, and breaks. The student registration fee excludes meals; traditionally, regular ASPLOS attendees who do not plan to use their meal tickets donate them to students.

Conference Site and Accommodation

All technical sessions, lunches, and registration will be held at the Fairmont Hotel. Conference rates are $107 per night for single or double room (10% city occupancy tax not included). Conference rates will be used if space is available.

The Fairmont Hotel is conveniently located in Downtown San Jose. It is adjacent to the city's light-rail transit line and is within walking distance of theaters, museums, civic buildings, and the Center of Performing Arts.

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